SPECIFICATION
FOR
LCM+CTP Module
KD035HVFMA065-C055A

MODULE:	KD035HVFMA065-C055A
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2019.10.12

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2019.10.12	V1.0	ALL	FIRST ISSUE

Contents

*** Description**

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorpho us silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit,back-light unit. The resolution of a 3.5'TFT-LCD contains 320x480 pixels, and can displa y up to 65K/262K colors.

*** Features**

-Low Input Voltage: 3.3V(TYP)

-Display Colors of TFT LCD: 65K/262K colors

-Interface: 8/9/16/18BIT MCU Interface

3/4SPI+16/18Bit RGB Interface

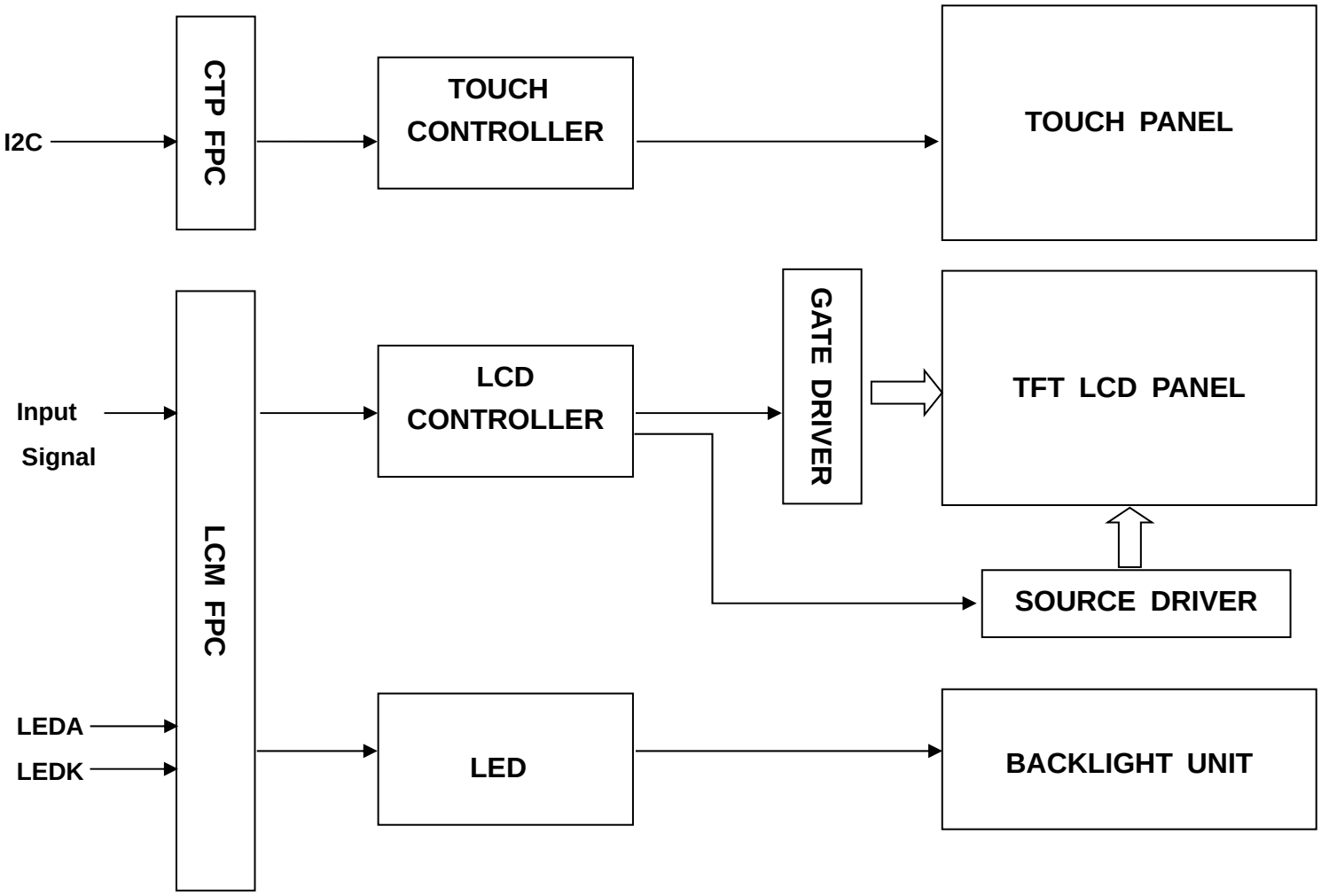
3-line/4-line serial interface

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	48.96(H)*73.44（V） (3.5inch)	mm	-
CTP View Area	50.96(H)*75.44（V）	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	320(RGB)*480	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153(H)*0.153(V)	mm	-
Viewing angle	ALL	o'clock	-
Controller IC	ILI9488	-	-
CTP Driver IC	FT5436	-	-
Display mode	Transmissive/ Normally Black	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

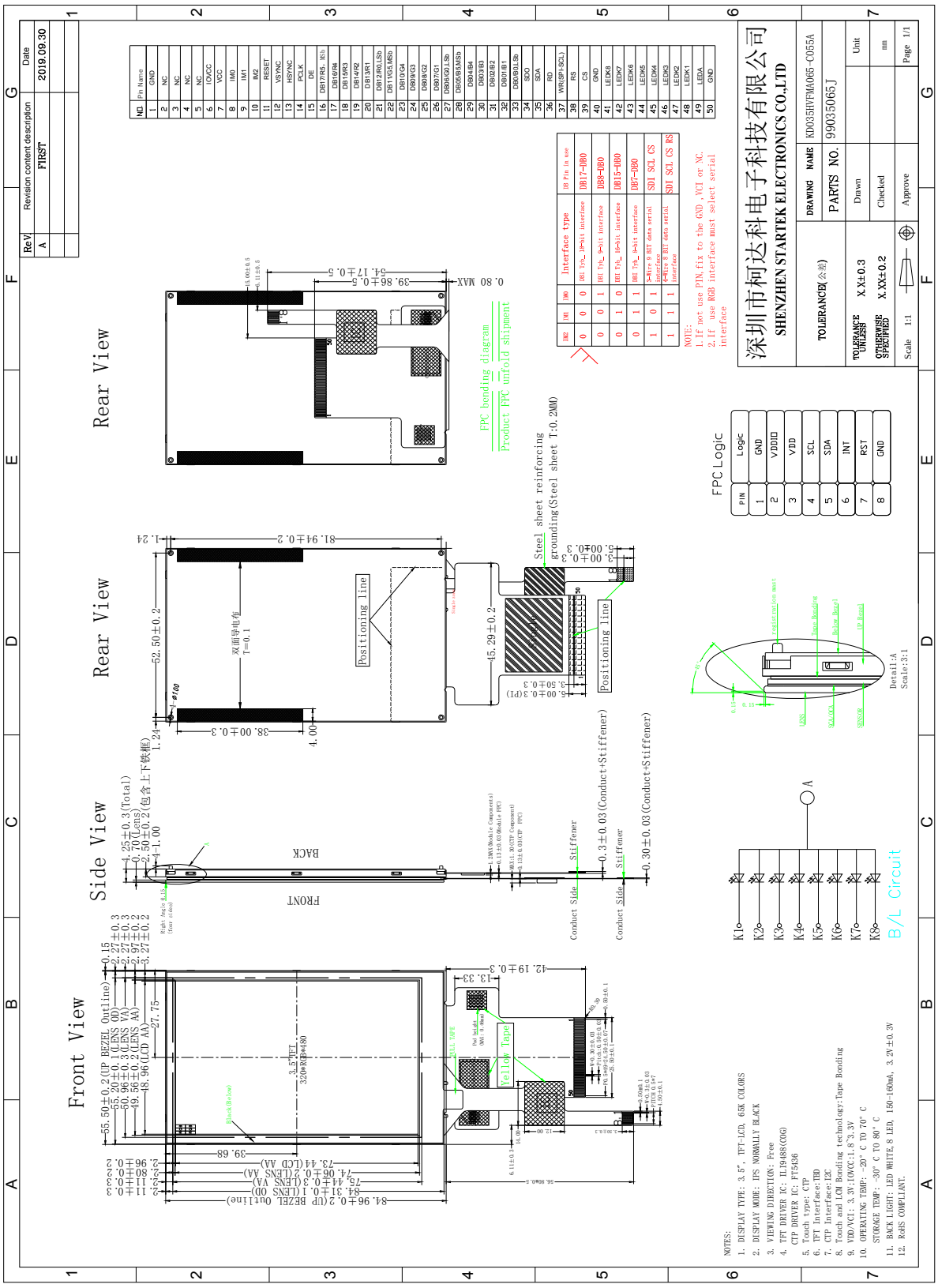
*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		55.5		mm	-
	Vertical(V)		84.96		mm	-
	Depth(D)		4.25		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

3.1 TFT

<table>
<tr><th>NO.</th><th>SYMBOL</th><th>DISCRIPTION</th><th>I/O</th></tr>
<tr><td>1</td><td>GND</td><td>Ground.</td><td>P</td></tr>
<tr><td>2</td><td>NC</td><td>NC</td><td></td></tr>
<tr><td>3</td><td>NC</td><td>NC</td><td></td></tr>
<tr><td>4</td><td>NC</td><td>NC</td><td></td></tr>
<tr><td>5</td><td>NC</td><td>NC</td><td></td></tr>
<tr><td>6</td><td>IOVCC</td><td>I/O power supply voltage.</td><td>P</td></tr>
<tr><td>7</td><td>VCC</td><td>Supply Voltage (3.3V).</td><td>P</td></tr>
<tr><td>8</td><td>IM0</td><td rowspan="3">Interface Selection
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface type</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Tyb_ 18-bit interface</td><td>DB17-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Tyb_ 9-bit interface</td><td>DB8-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Tyb_ 16-bit interface</td><td>DB15-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Tyb_ 8-bit interface</td><td>DB7-DB0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-Wire 9 BIT data serial interface</td><td>SDI SCL CS</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-Wire 8 BIT data serial interface</td><td>SDI SCL CS RS</td></tr>
</table></td><td rowspan="3">I</td></tr>
<tr><td>9</td><td>IM1</td></tr>
<tr><td>10</td><td>IM2</td></tr>
<tr><td>11</td><td>RESET</td><td>Reset input signal
Initialize the chip with a low input. Be sure to execute a power-on reset after supplying power.</td><td>I</td></tr>
<tr><td>12</td><td>VSYNC</td><td>Frame synchronizing signal
Fix to DGND level when not in use.</td><td>I</td></tr>
<tr><td>13</td><td>HSYNC</td><td>Line synchronizing signal
Fix to DGND level when not in use.</td><td>I</td></tr>
<tr><td>14</td><td>PCLK</td><td>Dot clock signal
Fix to DGND level when not in use.</td><td>I</td></tr>
<tr><td>15</td><td>DE</td><td>A data ENABLE input signal
Fix to DGND level when not in use.</td><td>I</td></tr>
<tr><td>16-33</td><td>DB17-DB0</td><td>18-bit data bus.
<table>
<tr><th>RGB Interface Type</th><th>Data PIN in Use</th></tr>
</table></td><td>I/0</td></tr>
</table>

		16 BIT RGB: DB0-DB15 18 BIT RGB: DB0-DB17 Fix to GND level when not in use	
34	SDO	Serial data output Leave the pin open when not in use.	O
35	SDA	DIN/SDA: serial data input/output bi-direction pin Fix to DGND level when not in use.	I
36	RD	serve as a read signal Fix to IOVCC level when not in use.	I
37	WR(SPI-SCL)	WRX pin, serves as a write signal SCL pin as Serial Clock when operates in the serial interface Fix to IOVCC level when not in use.	I
38	RS	Data/Command Selection pin Low: Command High: Parameter Fix to IOVCC level when not in use.	I
39	CS	Chip select input signal Low: the chip is selected and accessible High: the chip is not selected and not accessible Fix to IOVCC level when not in use.	I
40	GND	Ground.	P
41	LEDK8	Cathode pin OF backlight	P
42	LEDK7		
43	LEDK6		
44	LEDK5		
45	LEDK4		
46	LEDK3		
47	LEDK2		
48	LEDK1		
49	LEDA	Anode pin of backlight	P
50	GND	Ground.	P

3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	Supply voltage.（1.8-3.3V）	P
3	VDD	Supply voltage.(3.3V)	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	--	500	--		NOTE2
Response time	Rising	$T_{R+}T_F$		--	35	50	msec	NOTE4
	Falling							
Uniformity		S(%)		--	70	--	%	NOTE1
Color Filter Chromacicity	White	W_X		0.288	0.328	0.368		
		W_Y		0.348	0.388	0.428		
	Red	R_X		0.615	0.635	0.655		
		R_Y		0.317	0.337	0.357		
	Green	G_X		0.300	0.320	0.340		
		G_Y		0.615	0.635	0.655		
	Blue	B_X		0.137	0.157	0.177		
		B_Y		0.021	0.041	0.061		
Viewing angle	Hor.	Θ_L	CR>10	--	80	--		NOTE5
		Θ_R		--	80	--		
	Ver.	Θ_U		--	80	--		
		Θ_D		--	80	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

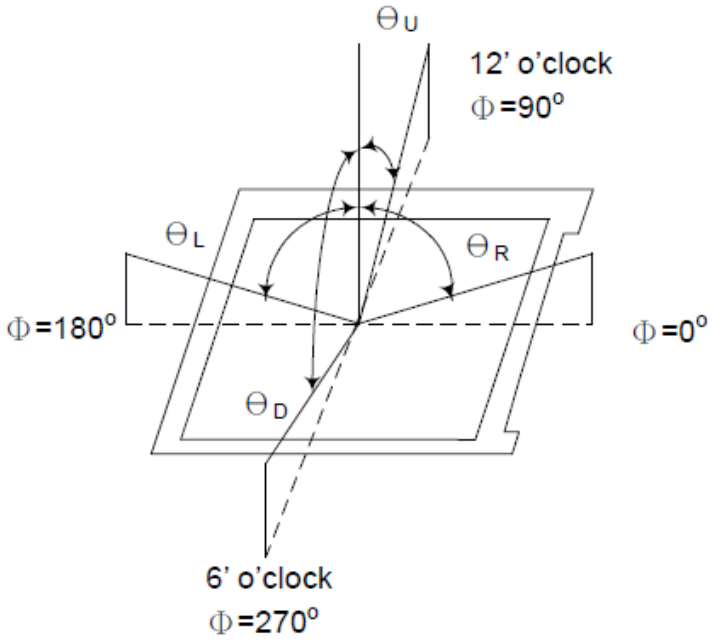
Ambient temperature : 25±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

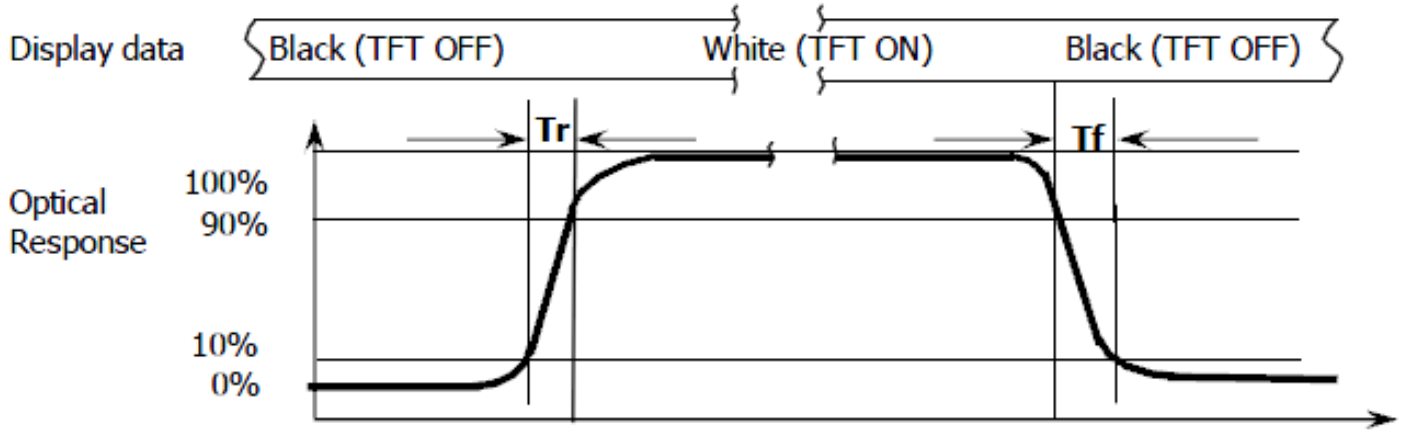
Note (1): Definition of Viewing Angle :



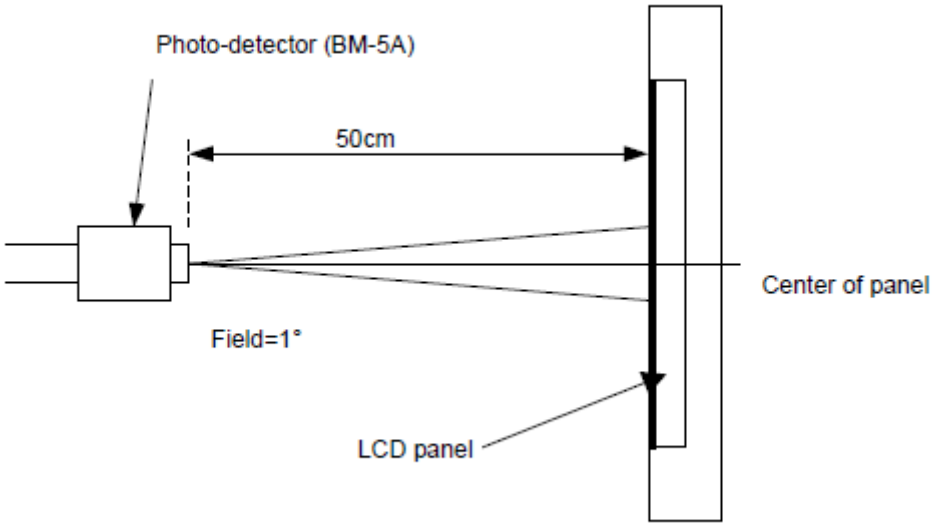
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCI	-0.3	3.3V	**V**
Digital interface supple Voltage	IOVCC	-0.3	3.3V	**V**
Operating temperature	T_{OP}	-20	+70	℃
Storage temperature	T_{ST}	-30	+80	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	3.3	V	
Digital interface supple Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current consumption	IDD	--	8	--	mA	
Level input voltage	V_{IH}	0.7IOVCC		IOVCC	V	
	V_{IL}	GND		0.3IOVCC	V	
Level output voltage	V_{OH}	0.8IOVCC		IOVCC	V	
	V_{OL}	GND		0.2IOVCC	V	

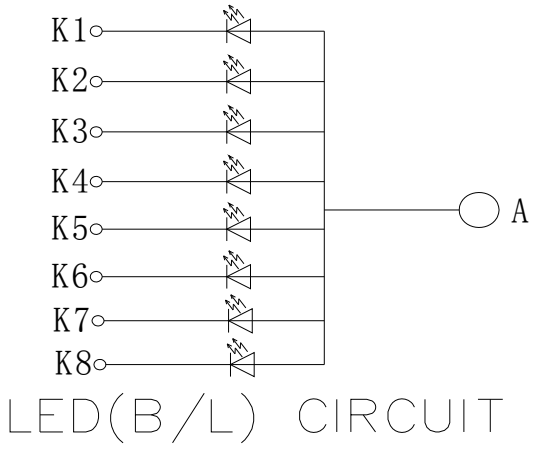
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 8 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	120	160	--	mA	
Forward Voltage	V_F	--	3.2	--	V	
LCM Luminance	L_V	290	340	--	cd/m2	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

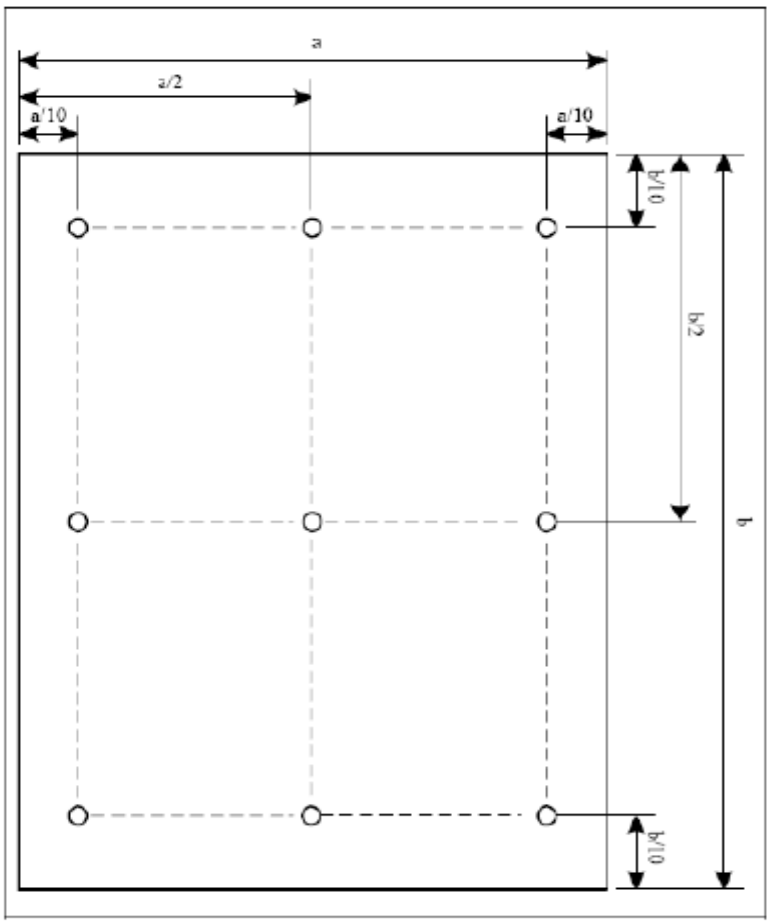
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=160mA. The LED lifetime could be decreased if operating IL is larger than 160mA. The constant current driving method is suggested.



LED(B/L) CIRCUIT

NOTE 3：Luminance Uniformity of these 9 points is defined as below:

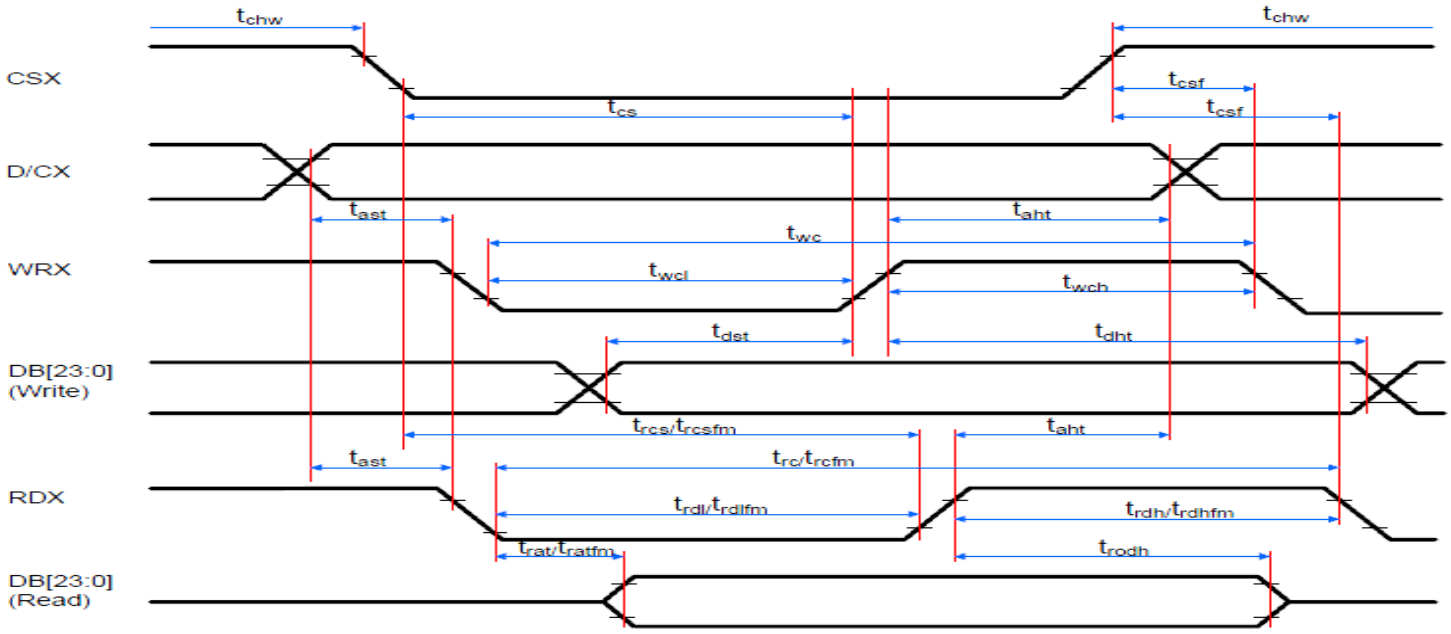


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. AC Characteristic

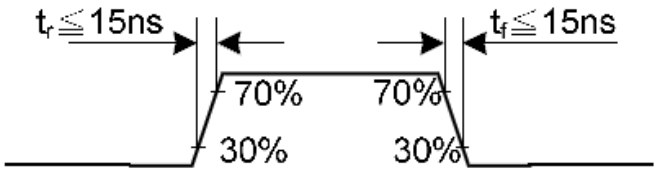
6.1 Display Parallel 8/16-bit Interface Timing Characteristics (8080 system)



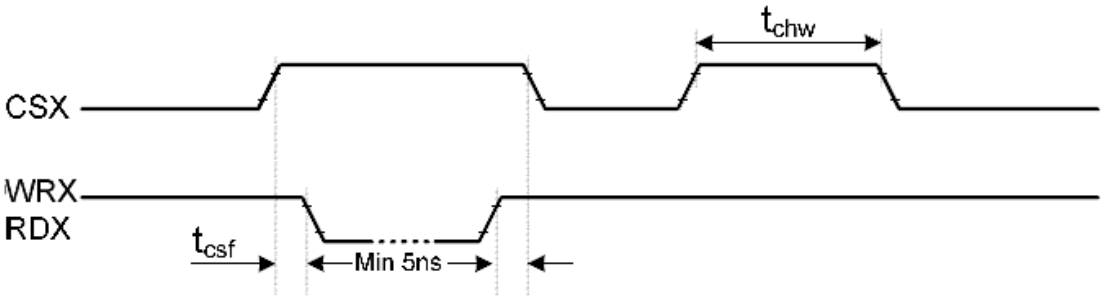
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	that	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Notes:

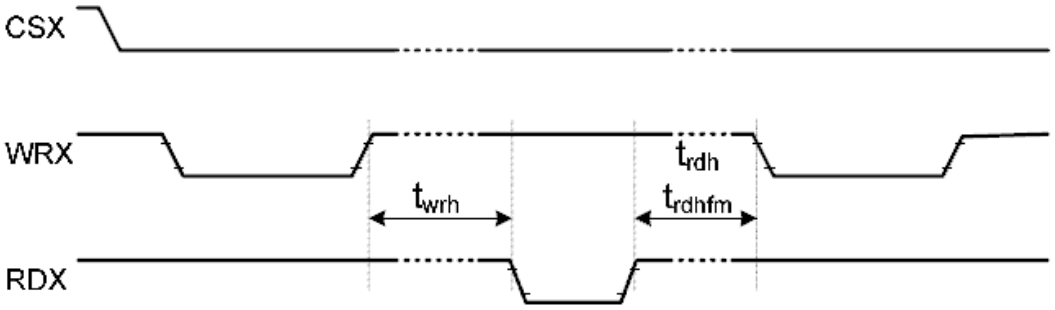
1. Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V
2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
3. Input signal rising time and falling time:



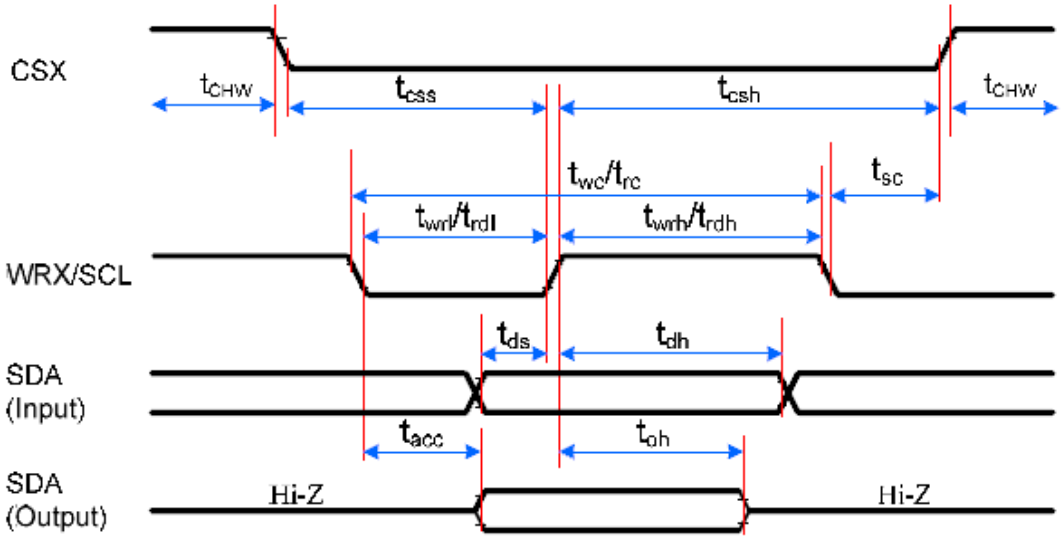
4. The CSX timing:



5. The Write to Read or the Read to Write timing:

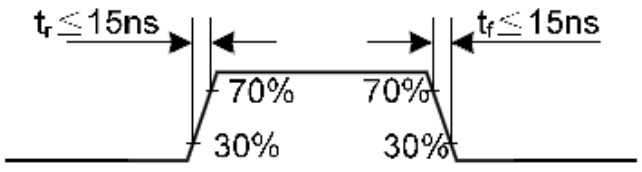


6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

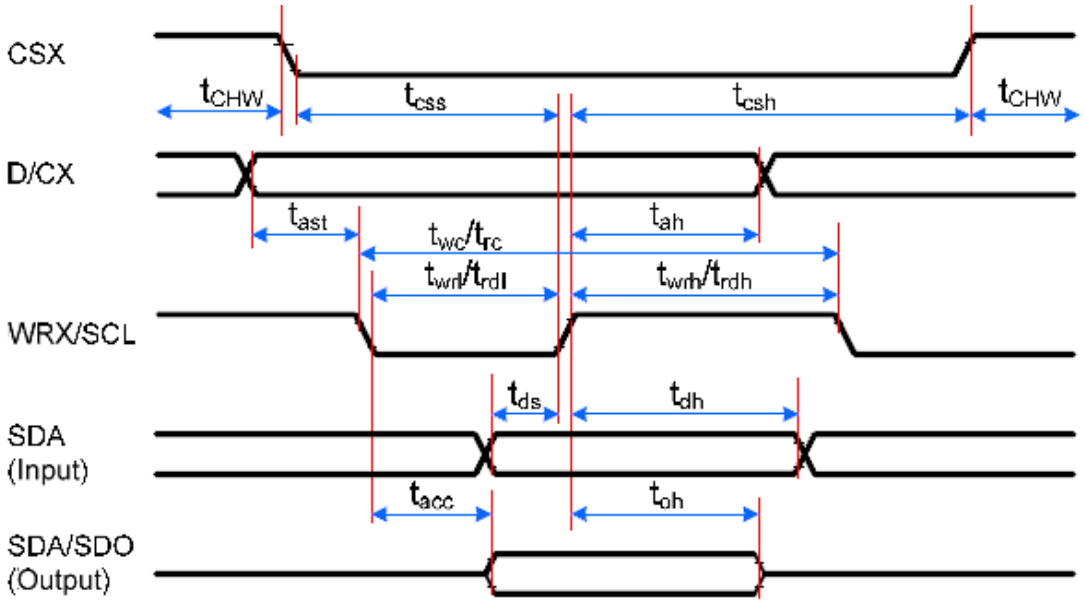


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



6.3 Display Serial Interface Timing Characteristics (4-line SPI system)

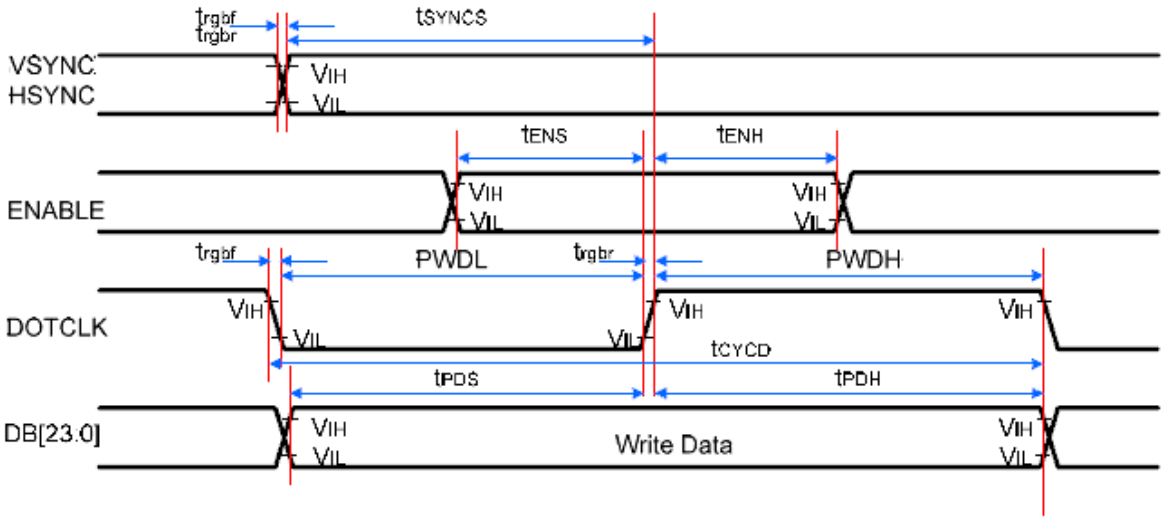


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	50	-	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
	twrl	SCL L pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Notes:

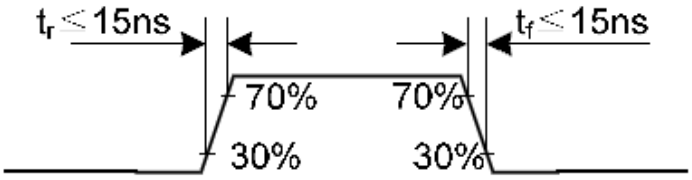
1. Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10+/-0.5ns.
2. Does not include signal rising and falling times.

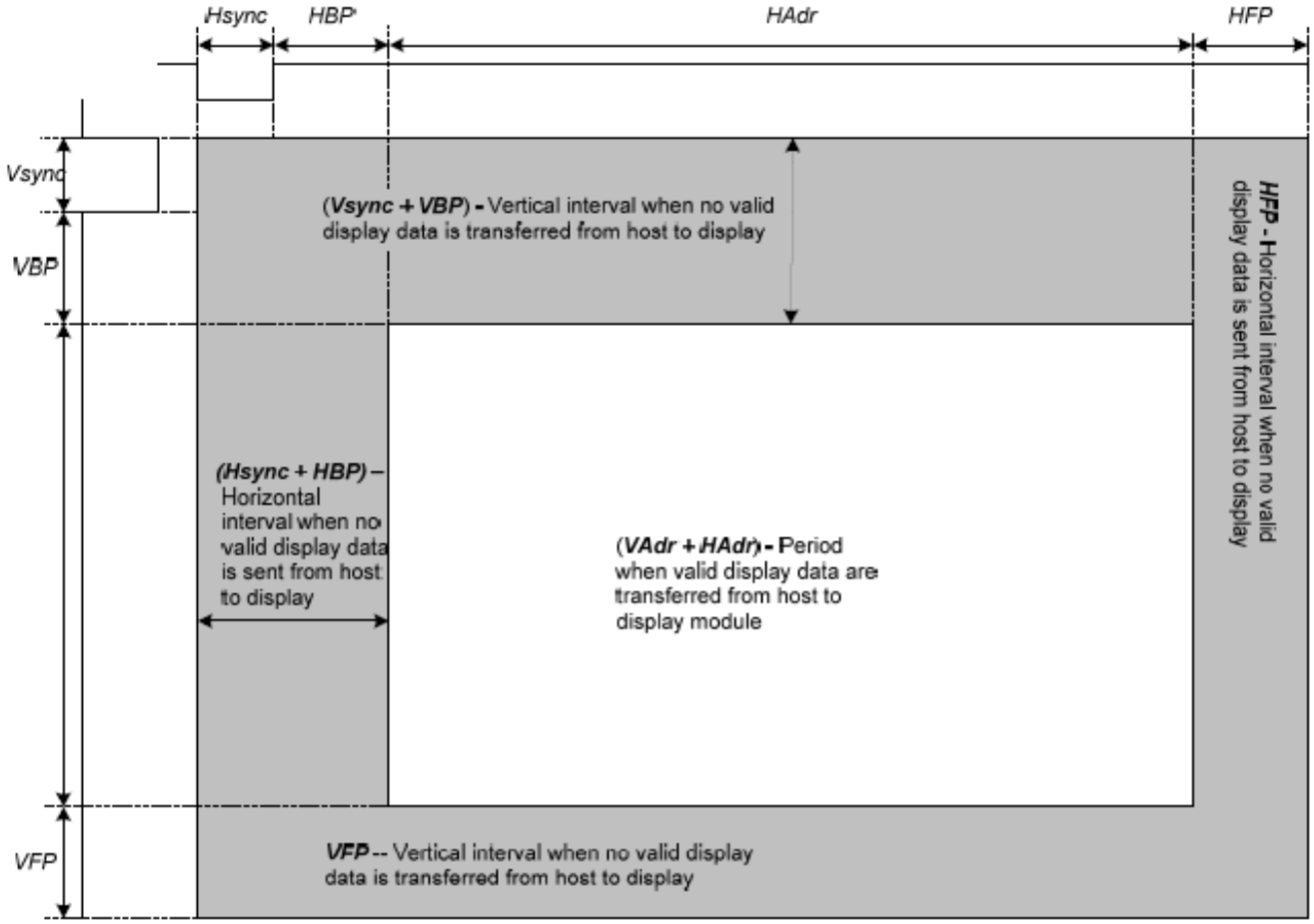
6.4 Parallel RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB [23:0]	t_{POS}	Data setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V





Parameters	Symbols	Min.	Typ.	Max.	Units
PCLK Cycle	$PCLK_{CYC}$	100	80	66.6	ns
Horizontal Synchronization	Hsync	3	3	-	PCLK
Horizontal Back Porch	HBP	3	3	-	PCLK
Horizontal Address	HAdr	-	320	-	PCLK
Horizontal Front Porch	HFP	3	3	-	PCLK
Vertical Synchronization	Vsync	2	2	-	Line
Vertical Back Porch	VBP	2	2	-	Line
Vertical Address	VAdr	-	480	-	Line
Vertical Front Porch	VFP	2	2	-	Line
Vertical Frequency(*)		50	60	80	Hz
Horizontal Frequency(*)		-	33	-	KHz
PCLK Frequency(*)		10	12.5	15	MHz

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

6.5 Reset Timing Characteristics

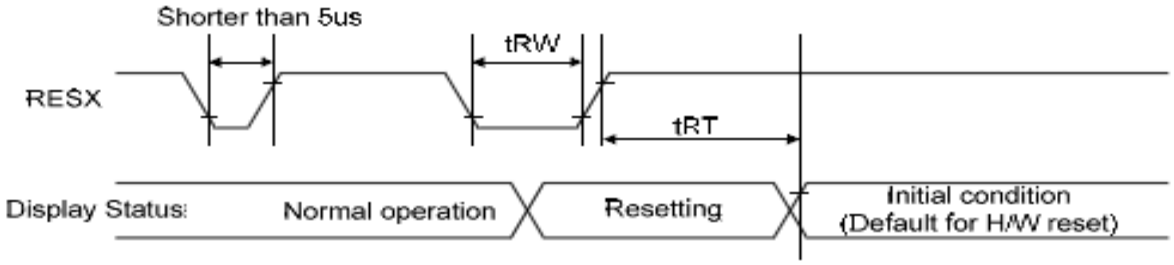


Table 39: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Table 40: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

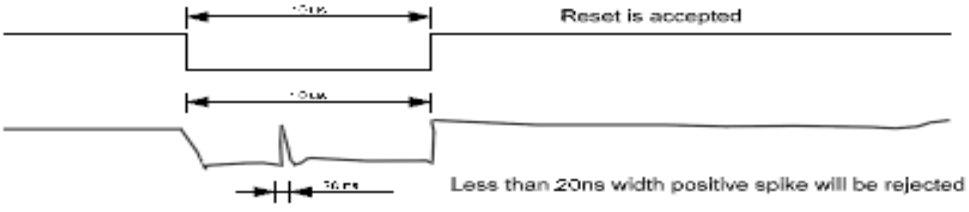


Figure 137: Positive Noise Pulse during Reset Low

7.CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.7	3.6	V	
Operating temperature	T_{OP}	-30	+85	℃	
Storage temperature	T_{ST}	-30	+85	℃	

7.1.2 DC Electrical Characteristics (Ta=25℃)

Item	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage/VDD	2.7	3.3	3.47	V	
Normal mode operating current	--	11	--	mA	
Sleep mode operating current	--	42	--	uA	
Monitor mode operating current	--	0.43	--	mA	
Digital Input low voltage/VIL	-0.3	--	0.3*VDD	V	
Digital Input high voltage/VIH	0.7*VDD	--	VDD	V	
Digital Output low voltage/VOL	--	--	0.3*VDD	V	
Digital Output high voltage/VOH	0.7*VDD	--	--	V	

7.1.3 AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V; Ta=25℃	49	50	51	

7.2 POWER ON/Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initia-lizing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

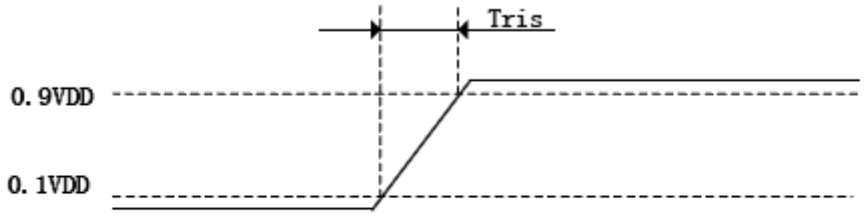


Figure 3-3 Power on time

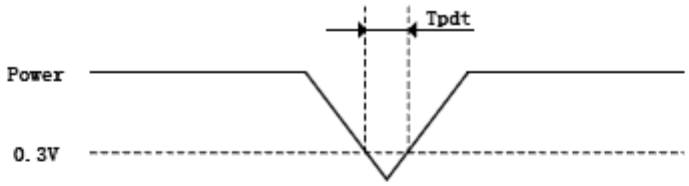


Figure 3-4 Power Cycle requirement

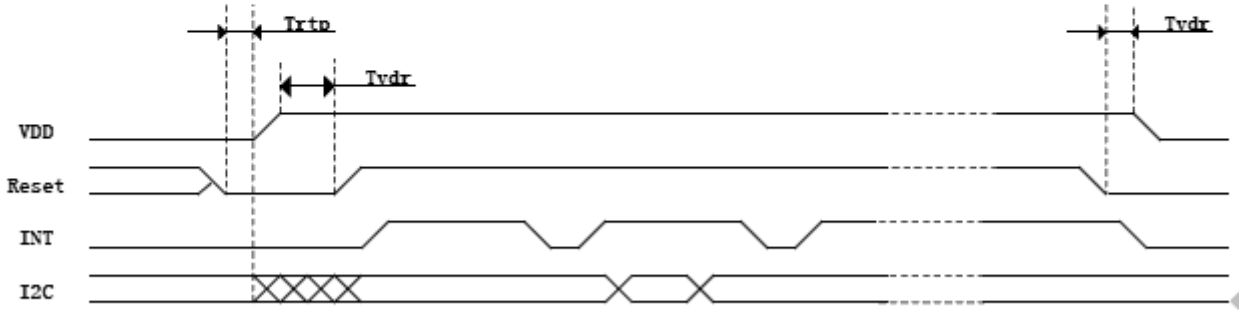


Figure 3-5 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

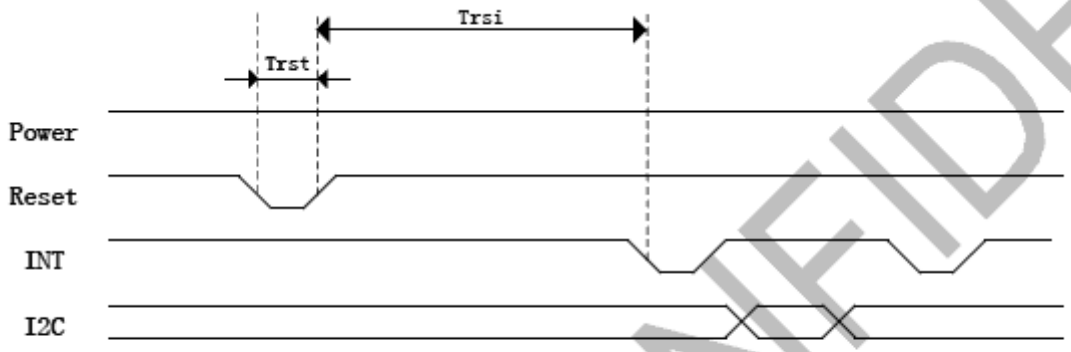


Figure 3-6 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	–	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	–	ms
Trtp	Time of resetting to be low before powering on	100	–	μs
Tvdr	Reset time after VDD powering on	1	–	ms
Trsi	Time of starting to report point after resetting	–	200	ms
Trst	Reset time	1	–	ms

7.3 I2C Timing

FT5436 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4.**

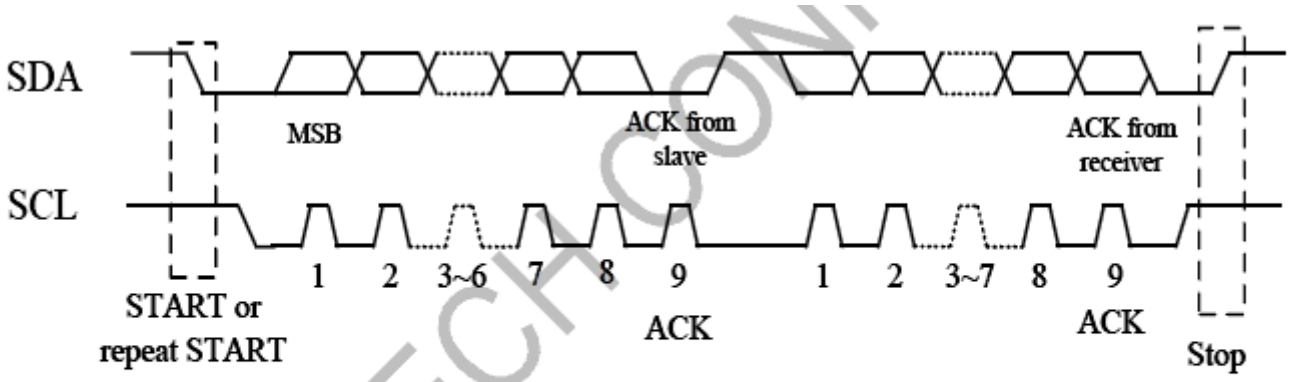


Figure 2-4 I2C Serial Data Transfer Format

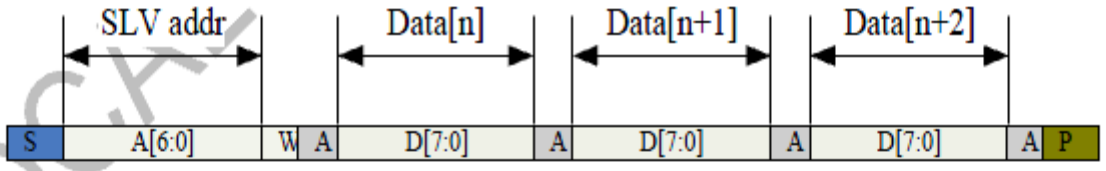


Figure 2-5 I2C master write, slave read

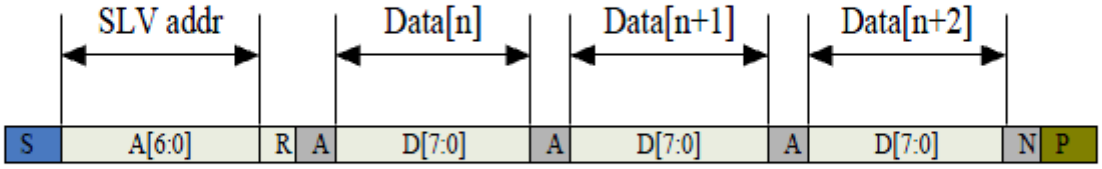


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

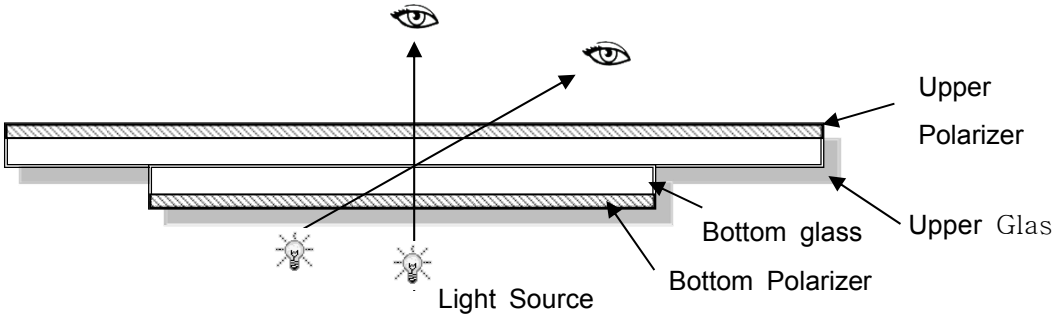
Temperature : 25±5℃

Humidity : 65%±10%RH

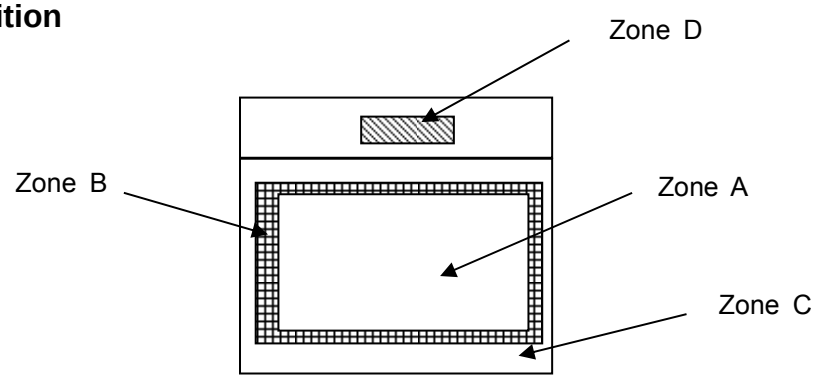
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C Cover (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:

As a general rule , visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

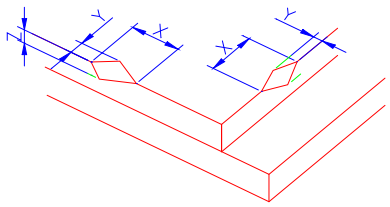
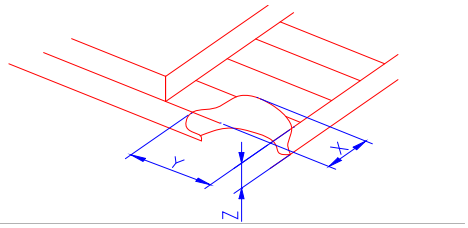
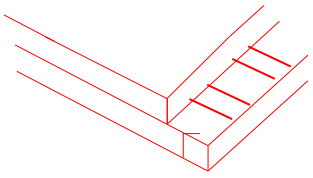
AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

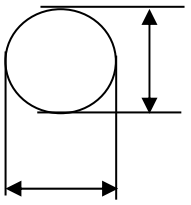
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot，Dim spot,Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

8.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

① light dot（LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.10	Ignore		Ignore
0.10<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.3	2		
Φ>0.35	0		

②Dim spot（LCD/TP/Polarizer dim dot, light leakage、dark spot）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.10<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.3	2		
Φ>0.35	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

④Pixel bad points（light dot，Dim dot, color dot）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.15<Φ≤0.25	2(distance≧10mm)		
Φ>0.3	0		

⑤ Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.4	3(distance≧10mm)		
0.5<Φ≤0.6	2		
0.6<Φ	0		

<table>
<tr><td>3.0</td><td>Line defect (LCD/ TP /Polarizer backlight black/white line, scratch, stain)</td><td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.07<W≤0.08</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>Electronic Components SMT</td><td>Not allow missing parts，solderless connection，cold solder joint，mis match，The positive and negative polarity opposite</td></tr>
<tr><td>5.0</td><td>Display color& Brightness</td><td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td></tr>
<tr><td>6.0</td><td>LCD Mura</td><td>By 5% ND filter invisible.</td></tr>
<tr><td rowspan="2">7.0</td><td rowspan="2">CTP Related</td><td>CTP Cover sensor accidented black/white spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.2</td><td colspan="2">3（distance≧10mm）</td></tr>
<tr><td>0.20<Φ≤0.25</td><td colspan="2">2</td></tr>
<tr><td>Φ＞0.3</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>CTP Cover scratch</td><td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Ignore (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="3">N≤3</td></tr>
<tr><td>0.07<W≤0.08</td><td>L≤3.0</td><td colspan="3">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
</table>

CTP Cover Pinhole/ Lack of ink

Zone / Size (mm)	Acceptable Qty
	C
Φ≤0.1	Ignore
0.1<Φ≤0.2	3(distance≧10mm)
0.25<Φ≤0.3	2
Φ>0.35	0

CTP Bonding bubble/ accidented spot

Size Φ(mm)	Acceptable Qty	
	A	B
Φ≤0.1	Ignore	
0.15<Φ≤0.2	3(distance≧10mm)	
0.2<Φ≤0.25	2	
Φ>0.25	0	

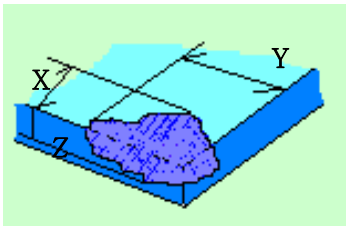
Assembly deflection

beyond the edge of backlight ≤0.2mm

TP cover broken
X：length
Y：width
Z：height

X	Y	Z
X≤0.5mm	Y≤0.5mm	Z<cover thickness

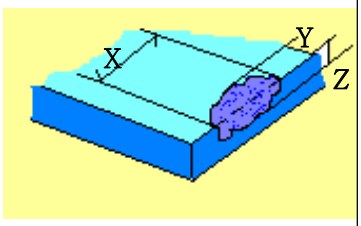
* Circuitry broken is not allowed.



TP cover broken
X：length
Y：width
Z：height

X	Y	Z
X≤0.3mm	Y≤0.3mm	Z<LCD thickness

* Circuitry broken is not allowed.



Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

9. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Storage	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10℃,30 min ↔ 60℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10. Cautions and Handling Precautions

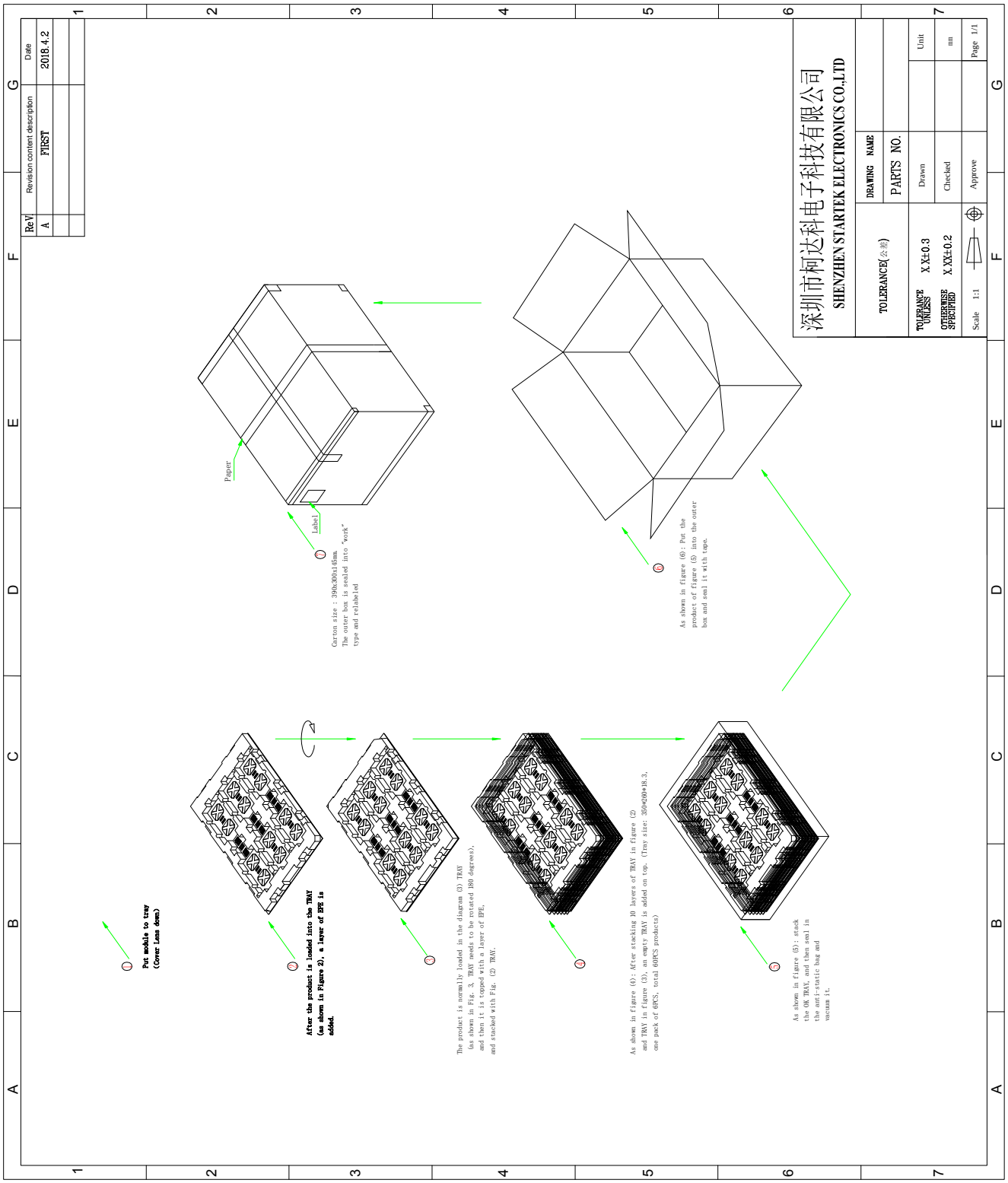
10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11. Packing


深圳市柯达科电子科技有限公司
SHENZHEN STARTEK ELECTRONICS CO.,LTD
Rev
A
Revision content description
FIRST
Date
2018.4.2
TOLERANCE(公差)
DRAWING NAME
PARTS NO.
Drawn
Checked
Approve
Unit
mm
Page 1/1
Scale 1:1
Paper
Label
Carton size : 390x300x145mm
The outer box is sealed into "work" type and relabeled
As shown in figure (6): Put the product of figure (5) into the outer box and seal it with tape.
Put module to tray
(Cover Lens down)
After the product is loaded into the TRAY
(as shown in Figure 2), a layer of EPE is added.
The product is normally loaded in the diagram (3) TRAY (as shown in Fig. 3, TRAY needs to be rotated 180 degrees), and then it is topped with a layer of EPE, and stacked with Fig. (2) TRAY.
As shown in figure (4): After stacking 10 layers of TRAY in figure (2) and TRAY in figure (3), an empty TRAY is added on top. (Tray size: 350*260*18.3, one pack of 60PCS, total 600PCS products)
As shown in figure (5): stack the OK TRAY, and then seal in the anti-static bag and vacuum it.